Amendments to the Claims:

1. (Previously amended) A wireless transmitter, comprising:

a plurality of antennas, wherein each of the plurality of antennas is operable for transmitting signals;

for each of a plurality of different user channels, circuitry for providing a plurality of groups of symbols in a first symbol group sequence;

for each of the plurality of different user channels, circuitry for forming a first modulated symbol group sequence for the user channel by modulating the symbols in the first symbol group sequence for the user channel with a unique code that corresponds to the user channel and distinguishes the user channel from each other of the plurality of different user channels;

circuitry for combining the first modulated symbol group sequence for each of the plurality of different user channels such that a first combined modulated symbol sequence is provided to and transmitted by a first antenna in the plurality of antennas;

for each of the plurality of different user channels, circuitry for forming a second symbol group sequence by time reversing symbols in at least some of the plurality of groups of symbols to form the second symbol group sequence different from the first symbol group sequence;

for each of the plurality of different user channels, circuitry for forming a second modulated symbol group sequence for the user channel by modulating the symbols in the second symbol group sequence for the user channel with a unique code that corresponds to the user and distinguishes the user from each other of the plurality of different user channels; and

circuitry for combining the second modulated symbol group sequence for each of the plurality of different user channels such that a second combined modulated symbol sequence is provided to and transmitted by the second antenna.

2. (Original) The wireless transmitter of claim 1 wherein the unique code used by the circuitry for forming a first modulated symbol group sequence is the same for a given user channel in the plurality of different user channels as the unique code used by the circuitry for forming a second modulated symbol group sequence.

3. (Original) The wireless transmitter of claim 1 wherein the unique code used by the circuitry for forming a first modulated symbol group sequence is time reversed for a given user channel in the plurality of different user channels relative to the unique code used by the circuitry for forming a second modulated symbol group sequence.

4. (Original) The wireless transmitter of claim 1 wherein the wireless transmitter further comprises circuitry for buffering a number of groups of symbols for each of the plurality of different user channels, wherein the number of groups of symbols equals the number of the plurality of antennas.

5. (Original) The wireless transmitter of claim 4 wherein the number of the plurality of antennas equals two antennas.

6. (Original) The wireless transmitter of claim 1 wherein the circuitry for forming a second symbol group sequence forms the second symbol group sequence further by determining a complex conjugate of the symbols in the first symbol group sequence.

7. (Original) The wireless transmitter of claim 6 wherein the circuitry for forming a second symbol group sequence forms the second symbol group sequence further by determining a negative of the symbols in selected groups of symbols within the first symbol group sequence.

8. (Original) The wireless transmitter of claim 1 wherein the transmitter is operable in a time division duplex mode.

9. (Original) The wireless transmitter of claim 8 code wherein each of the unique codes comprises a product of a Walsh code and a scrambling code, wherein each of the Walsh code and the scrambling code comprise a number of chips in a symbol.

10. (Original) The wireless transmitter of claim 9:
wherein the Walsh code consists of a number of chips and each symbol consists of a same number of chips as the number of chips in the unique code; and
wherein the unique code used by the circuitry for forming a first modulated symbol group sequence is time reversed for a given user channel in the plurality of different user channels relative to the unique code used by the circuitry for forming a second modulated symbol group sequence.

11. (Original) The wireless transmitter of claim 1 wherein the transmitter is operable in a frequency division duplex mode.

12. (Original) The wireless transmitter of claim 11 wherein each of the unique codes comprises a product of a Walsh code and a long code.

13. (Original) The wireless transmitter of claim 12:
wherein each group of the groups of symbols in the first symbol group sequence has a first number of chips;
wherein the long code consists of a second number of chips greater than the first number of chips; and
wherein the unique code used by the circuitry for forming a first modulated symbol group sequence is time reversed for a given user channel in the plurality of different user channels relative to the unique code used by the circuitry for forming a second modulated symbol group sequence by time reversing the first number of chips in the long code.

14. (Original) The wireless transmitter of claim 1 wherein the transmitter comprises a WCDMA transmitter.

Claims 15-27 (Previously canceled)

Claims 28-35 (Previously Canceled)

Claims 36-59 (Previously canceled)

60. (Currently amended) A circuit, comprising:

an input terminal coupled to receive a first and a second group of signals, each group having a respective sequence of different signals;

a first output terminal coupled to receive the first group of signals during a first time; and

a second output terminal coupled to receive a third group of signals having a sequence during the first time, the third group of signals comprising a same transform of each signal of the second group of signals, wherein the third group of signals is different from the second group of signals.

61. (Previously added) A circuit as in claim 60, wherein each signal of each group of signals comprises a symbol.

62. (Currently amended) A circuit as in claim ~~61~~ 60, ~~wherein each symbol is a quadrature phase shift keyed symbol~~ comprising a multiplier circuit arranged to multiply the first and third group of by first code.

63. (Previously added) A circuit as in claim 60, wherein the transform of the second group comprises conjugation and reversal of order in time.

64. (Previously added) A circuit as in claim 60, wherein the transform of the second group comprises conjugation, negation, and reversal of order in time.

65. (Previously added) A circuit as in claim 60, wherein the first output terminal is coupled to receive the second group of signals during a second time, and wherein the second output terminal is coupled to receive a fourth group of signals having a sequence during the second time, the fourth group of signals comprising a transform of the first group of signals.

66. (Previously added) A circuit as in claim 65, wherein the transform of the first group comprises conjugation and reversal of order in time.

67. (Previously added) A circuit as in claim 65, wherein the transform of the first group comprises conjugation, negation, and reversal of order in time.

68. (Previously added) A circuit as in claim 60, comprising a symbol mapper circuit having an input terminal coupled to receive a first sequence of data bits, the symbol mapper circuit producing the first and second groups of signals.

69. (Previously added) A circuit as in claim 68, wherein each signal corresponds to two of the data bits.

70. (Previously added) A circuit as in claim 68, comprising an interleaver circuit having an input terminal coupled to receive a second sequence of data bits, the interleaver circuit producing the first sequence comprising data bits of the second sequence having a different order.

71. (Previously added) A circuit as in claim 70, comprising a channel encoder circuit having an input terminal coupled to receive a third sequence of data bits, the channel encoder circuit encoding the third sequence to produce the second sequence of data bits.

72. (Previously amended) A circuit as in claim 71, wherein the channel encoder circuit encodes the third sequence of data bits with a convolutional code.

73. (Previously amended) A circuit as in claim 71, wherein the channel encoder circuit encodes the third sequence of data bits with a block code.

74. (Previously amended) A circuit as in claim 71, wherein the channel encoder circuit encodes the third sequence of data bits with a turbo code.

75. (Previously added) A circuit as in claim 60, wherein the first and second group of signals are encoded by one of a pseudo noise code, a Walsh code, and a combination of a pseudo noise code and a Walsh code.

76. (Previously added) A circuit as in claim 75, wherein the code applied to the second group of signals is reversed in time from the code applied to the first group of signals.

77. (Previously added) A circuit as in claim 75, wherein the first and second output terminals are arranged for connection to respective first and second antennas.

78. (Currently amended) A method of processing signals, comprising the steps of:

applying a respective ~~plurality~~ first and second group of signals to each of a plurality of encoder circuits, each first group of signals being different from each second group of signals;

producing each said respective first group ~~a first group of the respective plurality~~ of signals at a first output terminal of said each of a plurality of encoder circuits; and

producing a same transformation of each signal of said respective second group ~~transformed second group of the respective plurality~~ of signals at a second output terminal of said each of a plurality of encoder circuits~~; and modulating the first group and the transformed second group each of the respective plurality of signals by a respective code corresponding to said each of a plurality of encoder circuits.~~

79. (Previously added) A method as in claim 78, wherein each signal of the respective plurality of signals comprises a symbol.

80. (Currently amended) A method as in claim ~~79, wherein each symbol is a quadrature phase shift keyed symbol~~ 78, comprising modulating each said respective first group and each said transformation of each said respective second group of signals by a respective code corresponding to said each of a plurality of encoder circuits.

81. (Previously added) A method as in claim 78, wherein the transformed second group comprises conjugation and reversal of order in time of a second group of the respective plurality of symbols.

82. (Previously added) A method as in claim 78, wherein the transformed second group comprises conjugation, negation, and reversal of order in time of a second group of the respective plurality of symbols.

83. (Currently amended) A method as in claim ~~78~~ 80, comprising the steps of:

producing each said respective second group ~~a second group of the respective plurality~~ of signals at the first output terminal of said each of a plurality of encoder circuits;

producing a transformation of each said respective first group ~~transformed first group of the respective plurality~~ of signals at the second output terminal of said each of a plurality of encoder circuits; and

modulating each said respective second group and each said transformation of each said respective first group ~~the second group and the transformed first group each of the respective plurality~~ of signals by the respective code corresponding to said each of a plurality of encoder circuits.

84. (Previously added) A method as in claim 83, wherein the transformed second group comprises conjugation and reversal of order in time of a second group of the respective plurality of symbols, and wherein the transformed first group comprises conjugation, negation, and reversal of order in time of the first group of the respective plurality of symbols.

85. (Previously added) A method as in claim 78, comprising the steps of:

adding each said first group of the respective plurality of signals at each said first output terminal, thereby producing a first output signal; and

adding each said transformed second group of the respective plurality of signals at each said second output terminal, thereby producing a second output signal.

86. (Previously added) A method as in claim 85, comprising the step of encoding the first and second output signals with one of a pseudo noise code, a Walsh code, and a combination of a pseudo noise code and a Walsh code.

87. (Previously added) A method as in claim 86, wherein the code applied to the second output signal is reversed in time from the code applied to the first output signal.

88. (Previously added) A method as in claim 86, comprising the steps of:

applying the first output signal to a first antenna; and

applying the second output signal to a second antenna.

Claims 89-107 (Canceled)

108. (New) A method of processing signals, comprising the steps of:

receiving a first group of signals at an encoder circuit;

receiving a second group of signals different from the first group of signals at the encoder circuit;

producing the first group of signals at a first output terminal of the encoder circuit at a first time; and

producing a transformed second group of signals at a second output terminal of the encoder circuit at the first time, each signal of the transformed second group of signals having a same transformation.

109. (New) A method as in claim 108, wherein each signal of the first and second groups of signals comprises a symbol having plural bits.

110. (New) A method as in claim 109, wherein each symbol is a quadrature phase shift keyed symbol.

111. (New) A method as in claim 108, wherein each signal of the transformed second group of signals is a negative conjugate of a respective signal of the second group of signals.